

U.S. Patent Application Serial No. 10/659,337
Reply to Office Action dated May 21, 2004

AMENDMENTS TO THE SPECIFICATION:

Amend the specification as follows:

Please change the heading on page 1, line 8, from “[Field of the Invention]” to
Field of the Invention

Please change the heading on page 1, line 14, from “[Description of the Related Art]” to
Description of the Related Art

Replace the paragraph beginning at line 15, page 1, with the following rewritten paragraph:
Conventionally, a resin insulating film such as polyamide, BCB, or the like is generally used as a front face protective film for a chip mounted by mold, etc.

Replace the paragraph beginning at line 19, page 1, with the following rewritten paragraph:
An example of a chip using an insulating film such as polyamide, BCB, or the like as a front face protective film is shown in Fig. 8A to Fig. 8E. Fig. 8A and Fig. 8B are [[plane]] plan views showing a front face of the chip. Fig. 8C is a sectional view taken along the V-V line in Fig. 8B. Fig. 8D is a sectional view taken along the VI-VI line of Fig. 8B. Fig. 8E is a bottom view showing a reverse face of the chip.

Replace the paragraph beginning at line 5, page 2, with the following rewritten paragraph:

The upper side of the operating layer of the semiconductor is covered with a surface protective insulating film 105, such as polyamide, etc. A view in Fig. 8A shows a specification in which only the upper side of the operating layer is covered with the surface protective insulating film 105. A view in Fig. 8B shows a specification in which all the regions except the respective pad areas 102 to 104 are covered with the surface protective insulating film 105. Thus, exposure of the electrodes and the semiconductor area on the front face of the chip is reduced so as to take a structure aiming for improvement of reliability.

Replace the paragraph beginning at line 23, page 2, with the following rewritten paragraph:

As described above, an insulating film such as polyamide, BCB, or the like is often used as a front face protective film of a conventional chip. However, a device using polyamide or BCB cannot be utilized for an application which requires a high reliability. For example, polyamide has a high water absorbing property and would be saturated with absorbed water in the long term. Then, the water would be soaked out up to fingers such as the gate, the source, and the like to induce corrosion, ion migration, and so on. Therefore, there could be a risk of causing a malfunction in the device ~~trouble~~. On the other hand, BCB ~~is said to have~~ has an extremely small water absorbing property. However, the interface between metal and BCB, and BCB itself would be permeated with water. Therefore, there could be a risk of causing the aforementioned trouble.

Replace the paragraph beginning at line 11, page 2, with the following rewritten paragraph:

~~Due to~~ As a result of the above-described problems related to moisture resistance, a highly airtight hermetic seal package is used for a device which requires higher reliability. However, a hermetic seal package is extremely expensive and in some cases it costs several times as much as a chip.

Replace the paragraph beginning at line 13, page 4, with the following rewritten paragraph:

A problem when covering the insulating film with metal is that metal is conductive. It is needless to say that the chip cannot work when formed by a usual electrode forming method because all exposed electrodes and pads, etc., will be short-circuit short-circuited. Consequently, in this invention a structure is adopted so that all the necessary electrodes are led out from the front face to the reverse face. In other words, the semiconductor device according to this invention includes a plurality of electrodes connected to an active region on the front face of the semiconductor chip, a resin insulating film provided on the aforementioned active region, a metal protective film covering all of the upper surface and the side surfaces of the aforementioned resin insulating film, and one or a plurality of electrical connecting portions of the reverse face provided at the reverse side of the aforementioned semiconductor chip, leading out at least one electric potential of the aforementioned plurality of electrodes to the reverse face.

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Replace the paragraph beginning at line 24, page 5, with the following rewritten paragraph:

Fig. 3 is a [[plane]] plan view illustrating a process of manufacturing the chip of the second embodiment;

Replace the paragraph beginning at line 15, page 6, with the following rewritten paragraph:

A chip of a first embodiment is shown in Fig. 1A and Fig. 1B. Fig. 1A is a [[plane]] plan view showing a front face of the chip and Fig. 1B is a bottom view of a reverse face of the chip.

Replace the paragraph beginning at line 19, page 6, with the following rewritten paragraph:

On an operating layer (an active region) of a semiconductor substrate, a source electrode 11, a gate electrode 12 and a drain electrode 13 composing a FET are formed in a shape of the teeth of a comb.

Replace the paragraph beginning at line 23, page 6, with the following rewritten paragraph:

A source via hole receiving pad 11A led out from the source electrode 11 is provided on the front face of the semiconductor substrate, while a source bonding pad 11B is provided on the reverse face. [[These]] The source via hole receiving pad 11A and the source bonding pad 11B are connected to each other through a via hole 11C. In other words, electric potential of the source electrode 11 is led out to the source bonding pad 11B on the reverse face.

Replace the paragraph beginning at line 3, page 7, with the following rewritten paragraph:

Similarly, 12A is a gate via hole receiving pad on the front face of the semiconductor substrate led out from the gate electrode 12, 12B is a gate bonding pad on the reverse face, and 12C is a via hole. As well, 13A is a drain via hole receiving pad on the front face of the semiconductor substrate led out from the drain electrode 13, 13B is a drain bonding pad on the reverse face, and 13C is a via hole.

Replace the paragraph beginning at line 7, page 8, with the following rewritten paragraph:

As described above, the metal film 15 ~~performs~~ serves as an upper surface protective film of the insulating film 14, while the fringe metal layer 16 ~~performs~~ serves as a side surface protective film of the insulating film 14. Therefore, the chip is so structured that all of the upper surface and the side surfaces of the insulating film 14 are covered with the metal protective films. Thereby, a significantly superior moisture resistance will be realized because exposed parts of both faces on the device are composed only of the semiconductor substrate or the metal which adheres strongly to this semiconductor substrate.

Replace the paragraph beginning at line 5, page 9, with the following rewritten paragraph:

(2) In a case that a certain electrode is connected to the metal protective film, if there are a plurality of these electrodes, for example, if there are a plurality of the electrodes such as the source

electrodes 11 shown in Fig. 1A, those plurality of electrodes on the same electric potential (a plurality of the source electrodes 11) may be connected to the metal protective film.

Replace the paragraph beginning at line 27, page 9, with the following rewritten paragraph:

These applied examples have the following effects. For example, in the applied examples (1) and (2), when the electrode which is connected to the metal protective film is ground electric potential such as ground, etc., an electromagnetic shield effect by the metal protective film can be obtained. [[Since]] Because a plurality of the electrodes are connected to the metal protective film especially in the applied example (2), heat release occurs through the metal protective film having a large superficies. Therefore, the heat release property can be improved. Additionally, in the applied example (4) a contact above the front face of the chip will be possible.

Replace the paragraph beginning at line 12, page 10, with the following rewritten paragraph:

A second embodiment corresponds to the aforementioned applied examples (1) and (2). Specifically the source electrode is connected to the metal protective film. A chip of the second embodiment is shown in Fig. 2A to Fig. 2E. Fig. 2A is a [[plane]] plan view showing a front face of the chip. Fig. 2B is a sectional view taken along the I-I line in Fig. 2A. Fig. 2C is a sectional view taken along the II-II line in Fig. 2A. Fig. 2D is a sectional view taken along the III-III line in Fig. 2A. Fig. 2E is a bottom view of a reverse face of the chip.

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Replace the paragraph beginning at line 23, page 10, with the following rewritten paragraph:

On an operating layer of a semiconductor substrate, a source electrode 21, a gate electrode 22, and a drain electrode 23 composing a FET are formed in a shape of the teeth of a comb.

Replace the paragraph beginning at line 27, page 10, with the following rewritten paragraph:

A gate via hole receiving pad 22A led out from the gate electrode 22 is provided on the front face of the semiconductor substrate, while a gate bonding pad 22B is provided on the reverse face. [[These]] The gate via hole receiving pad 22A and the gate bonding pad 22B are connected to each other through a via hole 22C.

Replace the paragraph beginning at line 4, page 11, with the following rewritten paragraph:

Similarly, a drain via hole receiving pad 23A led out from the drain electrode 23 is provided on the front face of the semiconductor substrate, while a drain bonding pad 23B is provided on the reverse face. [[These]] The drain via hole receiving pad 23A and the drain bonding pad 23B are connected to each other though a via hole 23C.

Replace the paragraph beginning at line 24, page 11, with the following rewritten paragraph:

Within the inner side of the fringe metal layer 26, polyamide, etc., as an insulating film 24 is applied and the gate electrode 22, the drain electrode 23, the gate via hole receiving pad 22A and the drain via hole receiving pad 23A are covered with the insulating film 24. Therefore, different

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electrodes are insulated from one another. However, only the source electrode 21 is exposed to the upper surface of the insulating film 24.

Replace the paragraph beginning at line 15, page 12, with the following rewritten paragraph:

It is noted that though although the electrodes 21 to 23 and the via hole receiving pads 22A and 23A actually cannot [[been]] be seen from the outside as they are covered with the metal film 25, they are shown in Fig. 2A for the purpose of illustration.

Replace the paragraph beginning at line 20, page 12, with the following rewritten paragraph:

As described above, the metal film 25 performs as an upper surface protective film of the insulating film 24 and the fringe metal layer 26 performs as a side surface protective film of the insulating film 24. Therefore, the chip is [[so]] structured such that all of the upper surface and the side surfaces of the insulating film 24 are covered with the metal protective films and a significantly superior moisture resistance can be realized. Moreover, [[since]] because there is no need to lead out the source electrode 21 to the reverse face of the semiconductor substrate, the source via hole receiving pad and the source bonding pad described in the first embodiment will not be needed. Therefore, similarly to the chip having the source via hole structure described in the conventional example, it becomes possible to mount the chip by utilizing the reverse face to the bonding face of the gate and the drain (that is, the face with the metal protective film) as ground of the source. In addition, [[since]] because the metal film 25 above the front face of the chip can be flattened, it

becomes possible to mount the chip easily on the device where the main way of mounting is flip chip mounting.

Replace the paragraph beginning at line 15, page 13, with the following rewritten paragraph:

Referring to Fig. 2A to Fig. 6, a method of manufacturing the semiconductor device according to this embodiment will be explained hereinafter. Here, it will be explained by taking MESFET for instance, which is a compound semiconductor device using a GaAs substrate, etc., and has a high-frequency characteristic. Note that the same components as described in Fig. 2A to Fig. 2E will be explained with the same reference numerals and symbols in Fig. 3 to Fig. 6.

Replace the paragraph beginning at line 1, page 14, with the following rewritten paragraph:

Subsequently, as shown in Fig. 3, a gate electrode 22 is subjected to Schottky junction using metal such as Wsi, etc., and a source electrode 21 and a drain electrode 23 with an ohmic property using metal such as AuGe, etc., are formed in a shape of the teeth of a comb on the operating layer 30. An Au-plating layer with a film thickness of about $3 \mu\text{m}$ is formed for the ohmic metal to secure electric current density of the electrode.

Replace the paragraph beginning at line 15, page 14, with the following rewritten paragraph:

Thereafter, polyamide as the insulating film 24 is applied to [[whole]] all surfaces as shown in Fig. 4. Then, opening portions 28 are formed at the source electrode 21-1 and the fringe metal

layer 26-1 of the insulating film 24 to expose the upper surfaces of these source electrode 21-1 and fringe metal layer 26-1. As a process of making the openings, etching, etc., with chemicals using a photosensitive polyamide as the insulating film 24 may be performed.

Replace the paragraph beginning at line 24, page 14, with the following rewritten paragraph:

A source wiring 21-2 of the second layer and a fringe metal layer 26-2 of the second layer are then formed at the opening portions 28 by electrolytic Au plating as shown in Fig. 5. In other words, after forming the opening portions 28, metal is deposited on ~~the whole~~ all surfaces by a method such as sputtering, and then patterning is performed to make smaller areas than the opening portions 28 for plating. Subsequently, the Au-plating layer with a film thickness of about $4 \mu\text{m}$ is formed. By using this Au-plating layer as a mask, the metal which is deposited by a method such as sputtering should be removed by etching, such as milling method.

Replace the paragraph beginning at line 8, page 15, with the following rewritten paragraph:

Next, polyamide as the insulating film 24 is applied to the whole surfaces as shown in Fig. 6A and Fig. 6B. Fig. 6A is a sectional view taken along the IV-IV line in Fig. 6B. Then, opening portions 29 are formed at the source electrode 21-2 (the source wiring of the second layer) and the fringe metal layer 26-2 to expose the upper surfaces of these source electrode 21-2 and fringe metal layer 26-2. At this time as shown in Fig. 6B, only the upper surface of the source electrode 21-2 (the

source wiring of the second layer) is exposed to the front face of the chip inside the fringe metal layer 26-2, while other electrodes 22, 23 and pads 22A, 23A are covered with the insulating film 24.

Replace the paragraph beginning at line 22, page 15, with the following rewritten paragraph:

Thereafter, metal such as Ti or Ni, etc., are deposited on the whole surfaces by a method such as sputtering. Then, patterning is performed with resist so as to make a rectangular opening slightly inside of the chip region (inside of the outer edge of the fringe metal layer 26) above the transistor region which includes the fringe metal layer 26 and the gate electrode 21. Subsequently, an Au-plating layer with a film thickness of about $3 \mu\text{m}$ is formed and the resist is removed. As described above, the metal film 25 is formed as shown in Fig. 2B to complete the forming step of the front face of the substrate. The metal film 25 composing the metal protective film has a foundation layer of the sputtered metal and the Au-plating layer, so that adhesiveness to the insulating film 24 can be increased.

Replace the paragraph beginning at line 10, page 16, with the following rewritten paragraph:

Next, proceeding to the forming step of the reverse face of the substrate, the via holes 22C and 23C are formed from the reverse face of the semiconductor substrate 27 by dry etching, etc., as shown in Fig. 2C and Fig. 2E. Then, respective bonding pads 22B and 23B are plated with Au to complete the chip according to this embodiment.

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Replace the paragraph beginning at line 26, page 16, with the following rewritten paragraph:

Similarly to the second embodiment described above, a source electrode 31, a gate electrode 32, and a drain electrode 33 composing a FET are formed in a shape of the teeth of a comb on an operating layer of a semiconductor substrate.

Replace the paragraph beginning at line 3, page 17, with the following rewritten paragraph:

A gate via hole receiving pad 32A led out from the gate electrode 32 is provided on the front face of the semiconductor substrate, while a pad 32B (which is referred to as “a gate relay pad” hereinafter) is provided on the reverse face. [[These]] The gate via hole receiving pad 32A and the gate relay pad 32B are connected to each other through a via hole 32C.

Replace the paragraph beginning at line 11, page 17, with the following rewritten paragraph:

Similarly, a drain via hole receiving pad 33A led out from the drain electrode 33 is provided on the front face of the semiconductor substrate, while a pad 33B (which is referred to as “a drain relay pad” hereinafter) is provided on the reverse face. [[These]] The drain via hole receiving pad 33A and the drain relay pad 33B are connected to each other through a via hole 33C.

Replace the paragraph beginning at line 19, page 19, with the following rewritten paragraph:

In the aforementioned first to third embodiments the insulating films 14, 24, and 34 are covered with the metal films 15, 25 and 35 as the upper surface protective films, as well as they are

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covered with the hinge metal layer 16, 26, and 36 as the side surface protective films. Thereby strengthened metal protective films are formed. However, depending on the required reliability, after forming an insulating film, metal may be formed on ~~the whole~~ all surfaces of the insulating film at a time by sputtering, deposition, or the like without dividing the metal protective films into the upper part and the side part. Of course it can be considered that strength may be increased by Au-plating or the like on the once formed metal protective film. In this case, when the metal protective film which covers the resin insulating film terminates directly at a semiconductor substrate, an insulating film such as an SiO₂ film and an SiN film, or the like, reliability can be improved together with higher adhesiveness by using a foundation such as Ti, Ni, or the like, which has a superior adhesiveness.